AMENDMENTS TO THE CLAIMS

The following is a complete, marked-up listing of revised claims with a status identifier in parenthesis, underlined text indicating insertions, and strike through and/or double-bracketed text indicating deletions.

LISTING OF CLAIMS

1. (Previously Presented) A process for assembling at least one electronic component made up of a chip provided with contacts on one of the faces of the chip, said contacts being set off on a conductive film constituting flat conductive areas that extend the contacts of the chip in a plane over the chip, the conductive areas being connected to conductive tracks placed on a surface of a planar insulating substrate, comprising:

- placing the substrate on a work surface, the face including conductive tracks being oriented upwards,
- placing the electronic component into a cavity of the substrate situated in a zone including the conductive tracks, the chip being inserted into the cavity, the conductive areas of the electronic component coming into contact with the corresponding conductive tracks of the substrate, and
- applying a layer of insulating material which extends concurrently on the electronic component and at least on the zone of the substrate surrounding said electronic component, wherein the conductive areas of the electronic component and the conductive tracks of the substrate are in contact to achieve an electric connection via a pressure of application of the insulating material layer on the electronic component, and configured to rub together when repeated stressed are exerted on the substrate.

2. (Previously Presented) The process according to claim 1, wherein the electronic component is coated by an insulating material on the face of the chip opposite to the face provided with contacts.

3-5. (Cancelled)

6. (Currently Amended) The process according to claim 1, wherein the cavity ~~of the electronic component~~ is obtained by heating the chip of the electronic component, then pressing said chip into the substrate material so that the conductive areas of said electronic component are applied against the surface of the substrate.

7-8. (Cancelled)

9. (Currently Amended) The process according to claim 1 wherein the cavity ~~of the electronic component~~ is formed by milling or by stamping a window.

10-14. (Cancelled)

15. (New) A process for assembling at least one electronic component made up of a chip provided with contacts on one of the faces of the chip, said contacts being set off on a conductive film constituting flat conductive areas that extend the contacts of the chip in a plane over the chip, comprising:

placing a first substrate on a work surface,

placing the chip of the electronic component into a cavity of the first substrate, the conductive areas of the electronic component being applied against the surface of the first substrate, and

assembling the first substrate provided with the electronic component on a second substrate provided with conductive tracks, so that the conductive areas of the electronic component applied against the surface of the first substrate connect to the conductive tracks of the second substrate, wherein the conductive areas of the electronic component and the conductive tracks of the second substrate are in contact to achieve an electric connection via a pressure of application of the second substrate on the electronic component, and configured to rub together when repeated stresses are exerted on the substrates.

16. (New) The process according to claim 15, wherein the electronic component is coated by an insulating material on the face of the chip opposite to the face provided with contacts.

17. (New) The process according to claim 15, wherein the cavity is obtained by heating the chip of the electronic component then pressing said chip into the substrate material so that the conductive areas of said electronic component are applied against the surface of the substrate.

18. (New) The process according to claim 1, wherein the cavity is formed by milling or by stamping a window.

19. (New) A process for assembling at least one electronic component made up of a module including a set of flat contacts on one of the faces of the module, each contact of the set being linked with a contact area on the opposite face, comprising:

placing a first substrate on a work surface,

placing the chip of the electronic component into a cavity provided with a window cut into a first substrate with a thickness approximately equal to that of the module, the set of flat contacts shows on the surface level of said first substrate, and

assembling the first substrate provided with the electronic component on a second substrate provided with conductive tracks, so that the conductive areas of the opposite face of the electronic component connect to the conductive tracks of the second substrate, wherein the conductive areas of the electronic component and the conductive tracks of the second substrate are in contact to achieve an electric connection via a pressure of application of the second substrate on the electronic component, and configured to rub together when repeated stresses are exerted on the substrates.

20. (New) The process according to claim 19, wherein at least one module or a supplementary chip is mounted in one of the substrates, said module including conductive areas connected by pressure on the corresponding conductive tracks of either of the substrates.

21. (New) The process according to claim 20, further comprising a supplementary step of gluing and pressing the assembly formed by the superposition of the substrates.